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# Resistive switching memory device with metal-oxide quantum dots on a graphene layer

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We demonstrate a one diode–one resistor (1D–1R) type resistive switching memory device consisting of single layered metal-oxide quantum dots (QDs) and a vertically inserted graphene layer between the $SiO_2$ layers on an $n^+$-Si substrate. Mono-layered graphene on the bottom $SiO_2$ layer with a thickness of 50 nm was capped by a 5 nm thick $SiO_2$ top barrier layer deposited by using an ultra-high vacuum sputter. The $In_2O_3$ QDs layer embedded in the 50 nm thick biphenyltetracarboxylic dianhydride-phenylenediamine polymer layer was formed by a curing process using polyamic acid at 400 °C for 1 h. The current values of the high and low resistance states for this 1D–1R device were measured to be about $3.32 \times 10^{-9}$ and $5.54 \times 10^{-9}$ A at a read bias of 1 V, respectively. The ratio of each resistance after applying sweeping bias from +8 to −8 V and from −8 to +8 V appeared to be about 0.59 at 1 V. This resistance switching could have originated from the migration of the $O^{-2}$ ions by the redox chemical reaction in the polyimide and carrier charging effect of the QDs. This hybrid memory structure with $In_2O_3$ QDs and graphene layer has a strong possibility for application in next generation nonvolatile memory devices.



**1 Introduction** The device scale of flash memory is confronted with a quantum mechanical limitation. A nitride charge-trapped flash memory for commercial memory devices has been developed [1, 2]. However, next generation memory devices still require a breakthrough for the device scaling, the incensement of the density, and the reliability of multi-level cells [3]. Graphene is a critically important material for several fabrication issues in memory device and thin film transistor applications because single layered graphene have high mobility, mechanical flexibility, one atomic layer thickness, and versatile chemistry. In recent years, resistive switching memory devices have shown promising potential for application to various types of electronic devices, such as mobile smart phones, and wearable information technology devices [4, 5]. Furthermore, a resistive switching memory device conjugated with one diode and one resistor or one selector and one resistor has been reported. This achievement can improve the switching speed and suppress the snake current in cross–cross memory devices [6]. The field-effect tunneling device on the vertical graphene in the insulator reported that the tunneling coefficient of the hybrid structure with vertical graphene can be controlled by the Femi energy level at the vertical graphene layer [7]. In this study, we demonstrate a hybrid memory device with one diode and one resistor consisting of metal-oxide quantum dots (QDs) and the vertically inserted graphene layer between the $SiO_2$ tunnel barriers.

**2 Experimental** We fabricated hybrid memory structures consisting of QDs and mono-layered graphene, which was transferred to $SiO_2$ (50 nm)/highly doped $n^+$-Si substrate by using the polymethyl methacrylate coating method after being grown on Cu foil by chemical vapor deposition, as shown in Fig. 1. The 10 nm thick secondary $SiO_2$ layer for a diode structure was deposited on the mono-layered graphene by using an ultra-high vacuum sputtering system with a base pressure of about $1 \times 10^{-10}$ Torr. Also, indium with a thickness of 5 nm was deposited onto the secondary $SiO_2$ layer/sapphire substrate using a thermal

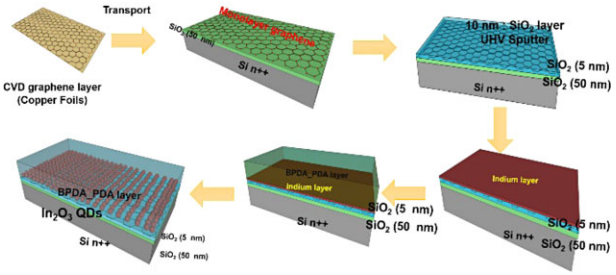


**Figure 1** Schematic illustration for the fabrication process of the 1D–1R resistive switching memory device consisting of metal-oxide QDs and vertically inserted graphene layer between the $SiO_2$ thin films on the high doped $n^+$-Si substrate.

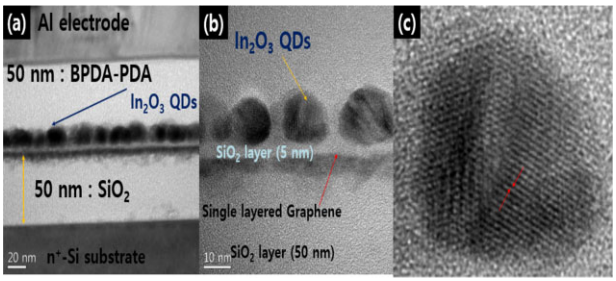


**Figure 3** The cross-sectional TEM images; (a) the resistive switching memory device, (b) $In_2O_3$ QDs with single layered graphene embedded in the $SiO_2$ tunnelling layer (5 nm) and 50 nm thick $SiO_2$ layer on the Si substrate, and (c) high-resolution TEM images of $In_2O_3$ QD in the BPDA-PDA polyimide layer.

evaporator. Then, 50 nm thick polyamic acid (PAA) was spin coated onto the deposited indium films. For formation of $In_2O_3$ QDs, biphenyltetracarboxylic dianhydride-phenylenediamine (BPDA-PDA) type PAA was used. The PAA solution was composed of BPDA-PDA in N-methyl-2-pyrrolidone (3 wt.%). During the indium dissolving process, the PAA and the indium were maintained at room temperature for about 24 h in vacuum desiccators. The $In_2O_3$ QDs were distributed on the secondary $SiO_2$ layer after chemical reaction between the indium layer and the PAA layer through soft baking at 125 °C for 30 min and a curing process at 400 °C for 1 h by using a furnace in $N_2$ ambient. The electrical properties for resistive switching memory devices with a graphene layer in Fig. 2 were evaluated by a current–voltage (*I–V*) measurement system with an HP4156A precision semiconductor parameter analyzer and a data acquisition system. The morphology of the $In_2O_3$ QDs and graphene layer were analyzed by using Tecnai G2 F30 (300 kV) field emission transmission electron microscopy (FE-TEM) at the Seoul Center for Korean Basic Science Institute.

**3 Results and discussion** After the chemical reaction between the indium film with a thickness of 5 nm and the BPDA-PAA layer, the FE-TEM images from the $In_2O_3$ QDs are shown in Fig. 3. The lattice fringe of the high resolution TEM images in Fig. 3(c) proves that the $In_2O_3$ QDs have a single crystalline structure. For identification of the composition of the $In_2O_3$ QDs between the $SiO_2$ layers on the graphene layer, energy dispersive X-ray spectroscopy (EDX) spectra were measured, as shown in Fig. 4. Then, several elements including O, Al, Si, and In appeared. Significantly, the element of In increased between 50 and 60 nm. According to the EDX spectra, the elements of the QDs after the post annealing process were conjugated with indium and oxygen. Also, the sputtered $SiO_2$ barriers for the secondary tunneling layer were found to be Si-rich $SiO_2$. As the results from the EDX showed, it appears that the single layered $In_2O_3$ QDs were distributed between the BPDA-PDA layer and the secondary $SiO_2$ layer to the trapping carriers for memory device application.

Figure 5(a) shows the *I–V* properties of the diode including the graphene monolayer without the $In_2O_3$ QD layers. It was expected to have similar electrical properties as the metal contact Schottky diode. However, it did not appear to have any resistive effect during the applied electric field. As a result, the $SiO_2$ layers, the vertically inserted graphene, and the BPDA-PDA layer could not create the condition pass by mobile ions. To evaluate the resistance switching effect of the

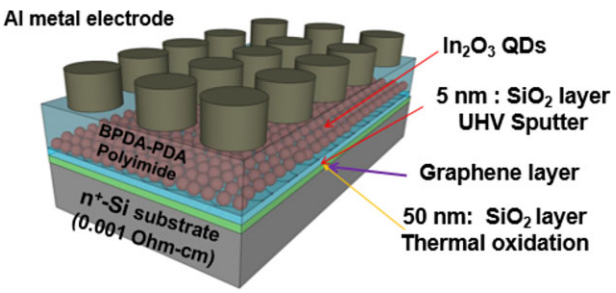


**Figure 2** The 3-dimensional schematic structure of the resistive switching memory device consisting of the $In_2O_3$ QDs on sandwiched graphene layer between the $SiO_2$ thin films on the highly doped $n^+$-Si substrate.

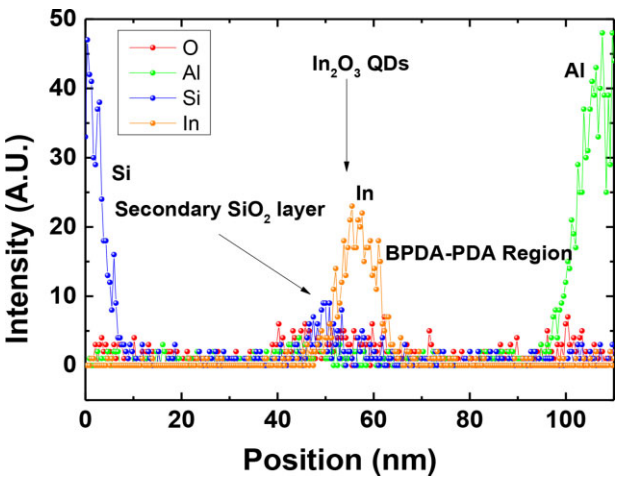


**Figure 4** The energy dispersive X-ray spectroscopy of the resistive switching memory device consisting of $In_2O_3$ QDs and graphene layer between the $SiO_2$ thin films.

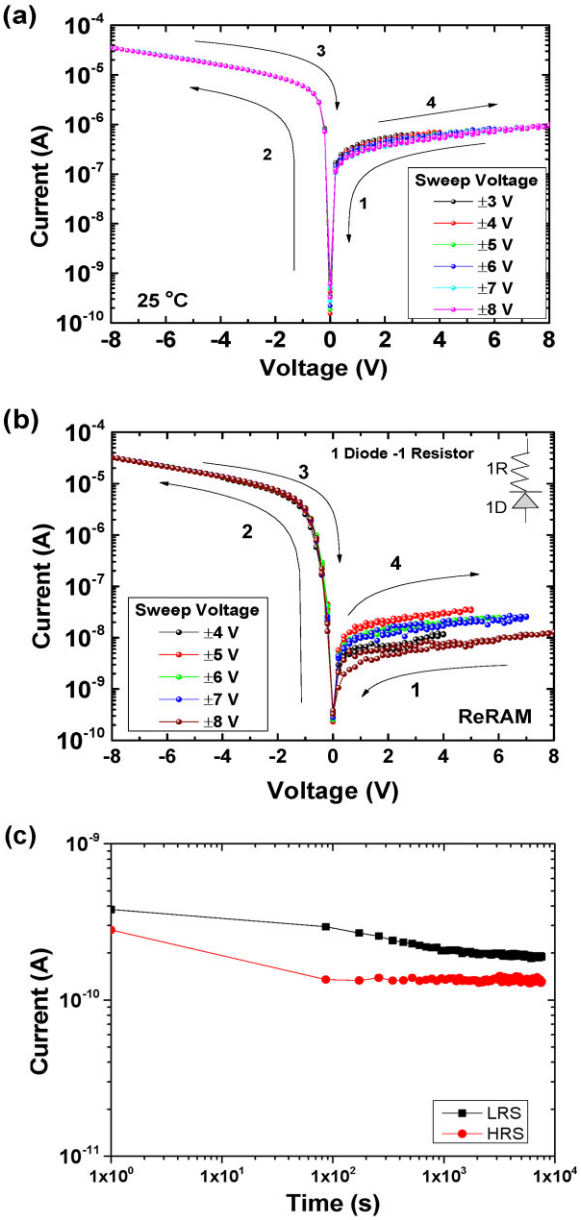


**Figure 5** *I–V* properties (a) without and (b) with the $In_2O_3$ QD layers of the memory device. (c) The retention properties at 1 V after applied positive and negative sweeping voltage from +8 to 0 V and from 0 to +8 V.

$In_2O_3$ QDs, the *I–V* characteristics were measured as shown in Fig. 5(b). After the bias voltage was applied from ±4 to ±8 V, the current levels in the positive bias region decreased from $10^{-7}$ to $10^{-9}$ A due to the Fermi level modulation of the graphene layer. Furthermore, when the sweeping voltage was applied from +4 to −8 V and from −4 to +8 V, current bistability appeared because of the effect of the carrier charging and discharging into the $In_2O_3$ QDs through the graphene layer and the oxygen ion drift-induced redox reactions at the BPDA-PDA polymer/$In_2O_3$ QDs interface. This indicates that the $In_2O_3$ QDs play a key role in determining the observed resistive switching phenomena. When a forward bias voltage is applied, negatively charged oxygen ions are created, leaving oxygen vacancies in the $In_2O_3$ QDs. These move away from the BPDA-PDA polyimide layer/$In_2O_3$ QDs interface boundaries. The current values of the high and low resistance states at 1 V of read bias for the 1D-1R device with $In_2O_3$ QDs and vertically inserted graphene were measured to be about $3.32 \times 10^{-9}$ and $5.54 \times 10^{-9}$ A, respectively. The ratio of each resistance after applying the sweeping bias from +8 to −8 V and from −8 to +8 V appeared to be about 0.59 at 1 V, as shown in Fig. 5(b). The retention properties at 1 V the 1D-1R device with $In_2O_3$ QDs after applied sweeping voltages from +8 to 0 V and from 0 to +8 V, as shown in Fig. 5(c).

The HRS/LRS showed a continuous decay of current level, simultaneity. The ratio of LRS/HRS after applying sweep bias was rapidly decreased from 0.59 to 0.1 after $10^4$ s. This degradation of retention could be correlated with the disconnection of the current path via generated O ions in BPDA-PDA layer and exchanged charge status in $In_2O_3$ QDs. The current conduction can be understood by fitting an *I–V* curve in a log–log scale. The carrier conduction mechanism during the bias voltage sweeping is shown in Fig. 6. The initial resistive switching behavior was caused by carrier trapping and the emission in the $In_2O_3$ QDs during the applied sweeping voltages. When the voltage was applied at a negative bias at the Al top gate electrode, the Fermi level of the graphene layer increased to the upper level of the Dirac-point energy level caused by modulation of the density of the states in the graphene layer. The carriers in the graphene were injected into $In_2O_3$ QDs through the first $SiO_2$ layer by applied positive voltage from 0 to 8 V and from 8 to 0 V. The slopes of the liner fitting of high resistance status (HRS) and low resistance status (LRS) were in a range from 0.40 to 0.61 [8–11]. Therefore, a possible reasonable conduction mechanisms through the secondary $SiO_2$ tunnel barrier could be affected by the trap assisted tunneling [12].

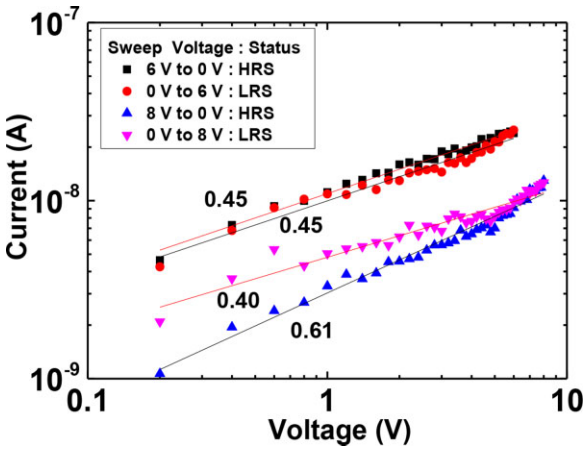


**Figure 6** The log (*I*)–log (*V*) plots of the non-volatile memory device with the metal-oxide QDs on sandwiched graphene monolayer between the $SiO_2$.

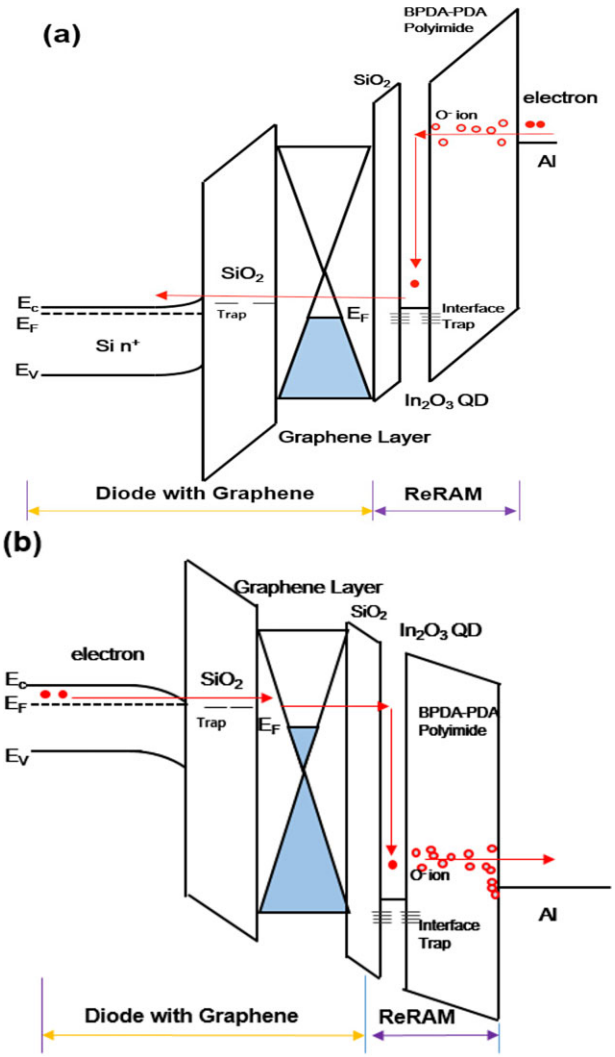


**Figure 7** Carrier transport mechanism of the resistive switching memory device after applying (a) negative (−) and (b) positive (+) bias at Al gate electrode. The device was combined by two parts of the diode with graphene and the ReRAM with $In_2O_3$ QDs and BPDA-PDA polyimide.

Figure 7 shows a schematic illustration of the band diagram for the memory device of the Al electrode/BPDA-PDA layer/$In_2O_3$ QDs layer/$SiO_2$ layer/graphene layer/$SiO_2$/$n^+$-Si substrate. The work functions of the $In_2O_3$ QDs and Al electrode were 4.3 and 4.08, respectively. The difference in the work function between the $In_2O_3$ QDs and $SiO_2$ layer created a quantum well structure. In this case, the Fermi level of the graphene layer was located at the Dirac-point by the equipment state as the zero bias. In addition, the electrons were trapped into the energy levels and the interface states of the $In_2O_3$ QDs. As mentioned above, the slope of the plotting log-$I$ versus the log-$V$ in Fig. 6 was about 0.40–0.45. The 0.60 of the HRS may have originated from the Ohmic conduction caused by the tunneling process. The dominant tunneling mechanism from graphene to Si n+ substrate is the trap assisted tunneling. The origin of the switching behavior was introduced mostly as the migration of the $O^{-2}$ ions for the redox chemical reaction in the polyimide and carrier charging effect of the QDs [13].

**4 Summary** This work presents 1D-1R resistive switching memory devices with $In_2O_3$ QDs on the sandwiched graphene monolayer between the $SiO_2$ thin films, and their electrical properties were evaluated for application of next generation non-volatile memory devices. The ratio of the current bistability of the hybrid memory device with the single-layered $In_2O_3$ QDs was found to be about 0.59 at 1 V when the bias voltage of ±8 V was applied. The electrical properties and transport mechanism for understating the memory effect were related with the quantum mechanical transport between the single-layered $In_2O_3$ QDs and the Fermi level of the graphene single layer through the modulated barrier height of the $SiO_2$ tunnelling layer.

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