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Toward negligible charge loss in charge injection memories based on vertically integrated 2D heterostructures

Dongri Qiu[1], Dong Uk Lee[2], Kyoung Su Lee[1], Sang Woo Pak[1], and Eun Kyu Kim[1] (✉)

[1] *Quantum-Function Research Laboratory and Department of Physics, Hanyang University, Seoul 04763, Republic of Korea*
[2] *NAND Development Division, NAND Product Engineering Group, SK Hynix, Icheon 17336, Republic of Korea*

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ABSTRACT

Two-dimensional (2D) crystals have a multitude of forms, including semi-metals, semiconductors, and insulators, which are ideal for assembling isolated 2D atomic materials to create van der Waals (vdW) heterostructures. Recently, artificially-stacked materials have been considered promising candidates for nanoelectronic and optoelectronic applications. In this study, we report the vertical integration of layered structures for the fabrication of prototype non-volatile memory devices. A semiconducting-tungsten-disulfide-channel-based memory device is created by sandwiching high-density-of-states multi-layered graphene as a carrier-confining layer between tunnel barriers of hexagonal boron nitride (hBN) and silicon dioxide. The results reveal that a memory window of up to 20 V is opened, leading to a high current ratio ($>10^3$) between programming and erasing states. The proposed design combination produced layered materials that allow devices to attain perfect retention at 13% charge loss after 10 years, offering new possibilities for the integration of transparent, flexible electronic systems.

1 Introduction

In the class of transition metal dichalcogenides (TMDs), semiconducting two-dimensional (2D) materials such as molybdenum disulfide (MoS_2) and tungsten disulphide (WS_2) have emerged as novel materials and have demonstrated various interesting physical properties [1, 2]. Combining semi-metallic graphene and the wide bang gap of hexagonal boron nitride (hBN) in van der Waals (vdW) heterostructures provides useful functionalities for electronic and optoelectronic applications including graphene-on-MoS_2 optoelectronic switches [3], vertically-encapsulated WS_2 tunneling transistors [4], and sandwiched ultra-thin hBN resonant tunneling devices [5]. A hybridized vdW system has also been utilized to create MoS_2- and black-phosphorus-based non-volatile memory devices by taking advantage of band diagram engineering for a

Address correspondence to ek-kim@hanyang.ac.kr

variety of 2D crystals [6–8].

Currently, many researchers have devoted significant effort toward building floating-gate memory cells with a high-κ dielectric-capped MoS_2 channel transistor via various charge-confining layers such as MoS_2 [6], multi-layered graphene (MGr) [9], hafnium oxide [10], metallic nanocrystals [11], and guanine [12]. Recent studies have confirmed that MGr with more than seven layers of graphene is favorable for use in floating gates, because the shift in the Fermi level of graphene with respect to the Dirac point is smaller than that of single-layer graphene under certain stored carrier densities [13, 14]. For constructing reliable data storage and a clearly defined write and erase states, tunnel barriers or insulators play a critical role. In particular, hBN is a perfect substrate without pinholes and is a gate dielectric with a dielectric constant of ε_{BN} = 3–4 [15] and a breakdown strength of ~8 MV/cm [15–17]. hBN is likely to replace conventional SiO_2 [18]. Additionally, WS_2 is an indirect-gap semiconductor (in bulk, E_g = 1.3 eV) [19–21] with an electron affinity of 4.0–4.4 eV [21, 22]. Although the atomic structure of WS_2 is similar to that of MoS_2, it is theoretically predicted to have the lightest effective mass [23], a high thermal stability [24], and a high chemical stability [25], which make it superior to other TMDs. Recently, Braga et al. have preliminarily shown that the density of defect states in the band gap of WS_2 is negligibly involved in its properties [4, 20]. Thus, WS_2 is likely to be suitable for use as a channel in memory cells; stable charged retention is expected because there are no available states for charge leakage via quantum mechanical tunneling. However, to our knowledge, floating-gate memory utilizing high-quality hBN with an incorporated WS_2 channel has not been studied.

The purpose of this work is to develop a novel concept for non-volatile memory in which MGr is sandwiched between the SiO_2 blocking layer and the hBN tunnel barrier to provide a deep potential well for electron trapping and detrapping. By integrating WS_2 as a channel material with multi-layered heterostructures, better retention than that of MoS_2 flash memory and strong hysteresis (up to 20 V) have been observed, because of the high charge storage capacity of MGr and high quality of WS_2 [4, 20, 26]. The experimental evidence demonstrates that vdW-heterostructure memory is capable of producing future non-volatile information storage devices.

2 Results and discussion

2.1 Preparation of MGr-embedded memory devices

Figure 1 shows the device architecture of the MGr embedded floating-gate memory device. The ternary heterostructures were atomically stacked on a 280-nm-thick SiO_2/Si substrate, for which a multi-layered WS_2 flake served as the field-effect channel, 9.5- to 25.7-nm-thick hBN was used as the tunnel dielectric. MGr acted as the charge-confining layer. Finally, degenerately-doped n^+-Si was utilized to control program/erase operations. Source/drain electrodes with a channel length of L = 3.5 μm and a width of W = 12.6 μm were patterned using a photolithography process and Ti/Au (20 nm/50 nm) metal thermal evaporation. All of the layered 2D materials were mechanically exfoliated from individual bulk crystals by applying the standard scotch-tape method, followed by a polydimethylsiloxane (PDMS)-based contamination-free transfer technique (more experimental details can be found in the Experimetanl section and the Electronic Supplementary Material (ESM), Section S1). An optical image of one of the investigated memory devices is shown in Fig. 2(a) (a corresponding Raman spectrum is presented in Fig. S2 in the ESM). Cross-sectional high-resolution transmission electron microscopy (HRTEM) was used to

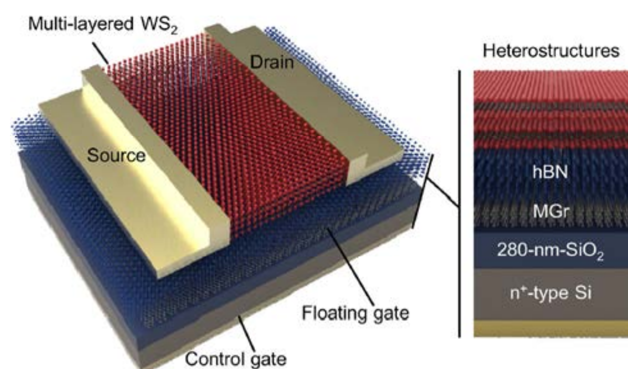

Figure 1 Schematic representation of a 2D crystal stacked memory device. Left: 3D view of the device layout. In this structure, ultra-thin hBN is precisely aligned on top of the pre-deposited MGr such that it overlaps with the WS_2 flake. Right: Schematic of the cross-sectional view of the device.

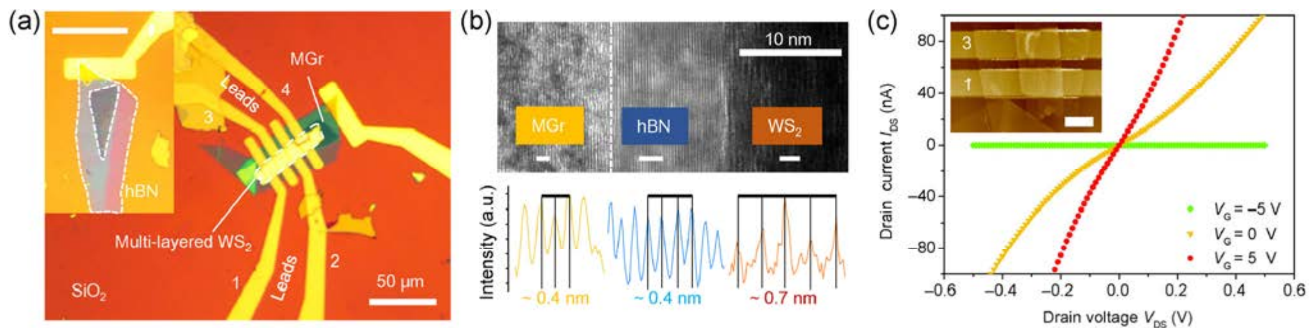

Figure 2 Characterization of the floating-gate memory device. (a) Optical image of a multi-layered WS_2 memory transistor. Inset: optical image of the device before metallization. The multi-layered graphene encapsulated by an hBN flake had a triangular shape for electrical isolation (the scale bar is 50 μm). Note that electrodes 1 to 3 lack underlying MGr. (b) Cross-sectional HRTEM image of the 2D stacks and non-normalized intensity profile along the highlighted (white) bar in the TEM image. The thicknesses of hBN and WS_2 were 12.7 and 17.1 nm, respectively. (c) Small drain voltage dependence of the current under different gate voltages (inset of Fig. S5 in the ESM). Inset: AFM image of the memory devices extracted from the device shown in (a) (the scale bar is 6 μm).

verify the interfacial flatness, layer thickness, and crystallinity of the WS_2–hBN–MGr stacks. As presented in Fig. 2(b), a clearly resolved HRTEM image demonstrated that the interfacial layer of the vdW stack is atomically sharp and free from contamination. The slightly different contrast between graphene and hBN allowed for the identification of the layer composition and thickness, which is in agreement with the atomic force microscope (AFM) characterization (see the inset of Fig. 2(c)). Details of the transmission electron microscopy (TEM) analysis, including scanning TEM and energy-dispersive X-ray spectroscopy (EDX), are provided in the ESM, Section S3.

2.2 Electrical performance of the heterostructured devices

Before determining the systematic electrical transport properties, a small drain voltage V_{DS} was applied between electrodes 1 and 3, and the drain current I_{DS} was measured (Fig. 2(a)). The I_{DS}–V_{DS} output curve shows nearly linear behavior and the presence of small Schottky barriers, acquired from various gate voltages V_G (Fig. 2(c)), similar to the results of previous reports [19, 27–29]. We assumed that the device has a sufficiently low MoS_2/metal contact resistance and that there is little influence on the device performance when we apply large voltages for electrical measurements. Figure 3(a) shows typical I_{DS}–V_{CG} transfer characteristics for a fabricated device. The direction of V_{CG} varied from a positive sweep (from −25 to +25 V) to a negative sweep (from +25 to −25 V), and a memory window ΔV of as large as ~20 V (defined as the amount of threshold voltage V_{TH} shift) was acquired. The measured ΔV as a function of maximum control gate voltage $|V_{CG,MAX}|$ is shown in the inset of Fig. 3(b). This strong hysteresis may originate from various charge-trapping mechanisms such as trapped charge at the hBN–WS_2 interface and charge capturing by adsorbates, i.e., moisture and oxygen [30]. Moreover, the presence of the band-tail states in the WS_2 system due to inhomogeneity and disorder also produced an increase in the V_{TH} shift [31]. However, this phenomenon was confirmed in two separate experimental cases, namely, changing the control gate sweep speed and removal of the charge-trapping layer. The resulting data verified that the remarkable counter-clockwise hysteresis was attributed to electron trapping in the embedded MGr layer (see the ESM, Section S4, for more detail). The field-effect transistor (FET) without underlying graphene was also measured via electrodes 1 to 3. In this structure, the WS_2 channel was positioned on the hBN substrate and exhibited n-type behavior with a high on/off current ratio of ~10^5 and a transconductance of 18.3 nS, which is consistent with results from a previous study (more evidence is shown in Fig. S5 in the ESM) [32–34].

Next, we studied the temporal retention property of the devices by employing the gate sweep voltage dependence of ΔV. As illustrated in Fig. 3(b), two distinct I_{DS} levels can be generated. The on-state occurs

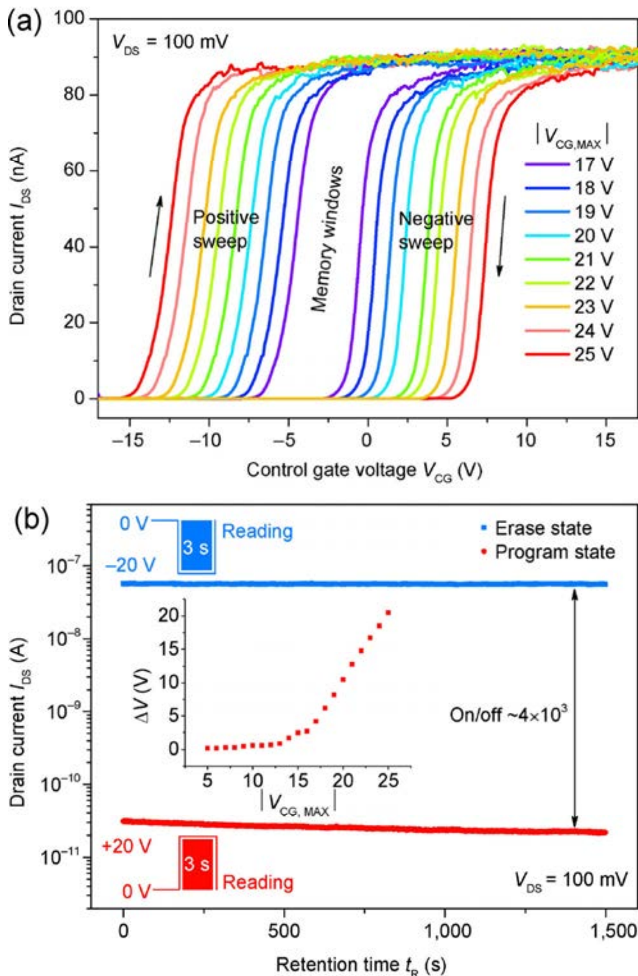

Figure 3 Electrical performance of the memory devices. (a) I_{DS}–V_{CG} transfer characteristics of the device acquired using positive and negative voltage sweeps at V_{DS} = 100 mV. The maximum control gate voltage changes from 5 to 25 V. (b) Evolution of temporal retention characteristics after applying ±20 V for a Δt = 3 s pulse with an erase/program state ratio of 4×10^3 for a t_R = 1,500 s retention time. Inset: memory window as a function of maximum control gate voltages extracted from data in (a).

upon applying an erase voltage pulse of $V_{CG,E}$ = –20 V with a pulse duration Δt of 3 s. A reverse programming voltage $V_{CG,P}$ = +20 V with the same Δt corresponds to the off-state of the device. In this measurement, the readout voltage was set to V_{CG} = 0 V. This semi-permanent current level was attributed to the V_{TH} shift, which is due to confined charges in the floating-gate; this shift did not release charges, which leads to a non-volatile memory effect. Most of the prepared devices in this work exhibited similar memory properties with a high on-/off-state ratio of approximately 10^3, and maintained a retention time t_R of greater than 1,500 s, regardless of the thickness of the tunnel dielectric (see Fig. S6 in the ESM).

2.3 Electrical conduction in the tunnel dielectric

The basic operation principle of the proposed memory device is the storage (programming) or removal (erasing) of electrons in the electrically isolated floating gate when applying a pulse from the outside. This programming and erasing sequence of the floating-gate memory can be understood using an energetic band diagram (Fig. 4(b)). The mechanism of carrier transport (or charge injection) through a thin tunnel barrier, in this case, is generally referred to as electrode-limited conduction [35], where we assume that the bottom dielectric (SiO_2) is ultimately blocked. The MGr has a similar work function to graphite, given as 4.6 eV [36], with a value of $e\chi_{BN} \approx 2.0$ eV for the electron affinity of hBN [6, 7, 37]. Therefore, after bringing MGr and hBN into contact with each other, the tunnel barrier height $e\phi_{BE}$ at their interface can be roughly estimated as being larger than 2.5 eV using Anderson's rule when the charge redistribution effect (which leads to band bending) is neglected.

To evaluate ϕ_{BE}, we also created Ti–WS_2–hBN–MGr–Ti stacks (Fig. 4(a)) for measuring the tunneling current. Figure 4(c) presents the current density J_B transport through a 21-nm-thick hBN barrier as a function of the applied voltage V_B. Two modes of the electrical conduction mechanism were revealed in the forward-bias-associated curve (Fig. 4(c)). Qualitatively, if the voltage drops on the hBN dielectric satisfies $V_{BN} < \phi_{BE}$, then direct tunneling occurs. Beyond this critical point, i.e., $V_{BN} > \phi_{BE}$, electrons will encounter a triangular barrier and Fowler–Nordheim (F–N) tunneling will occur [38]. This current density in the F–N tunneling regime, when neglecting the second-order effect, can be expressed as $J_{FN} = C_1 F_{BN}^2 \exp[-(32m_{BN}^*)^{1/2}(e\phi_{BE})^{3/2}/3\hbar e F_{BN}]$, where, F_{BN}, $\hbar$, and e are the electric field in the dielectric, Plank's constant, and the elementary charge, respectively [38–40]. The F–N plot is illustrated in Fig. 4(d), where the intercept of the line gives the value of C_1, where C_1 is given by $e^2/16\pi^2\hbar\phi_{BE}(m_e/m_{BN}^*)$, m_e is the free electron mass and m_{BN}^* = 2.21m_e is the effective mass of hBN [41]. Therefore, the tunnel barrier for electrons at the MGr–hBN interface was

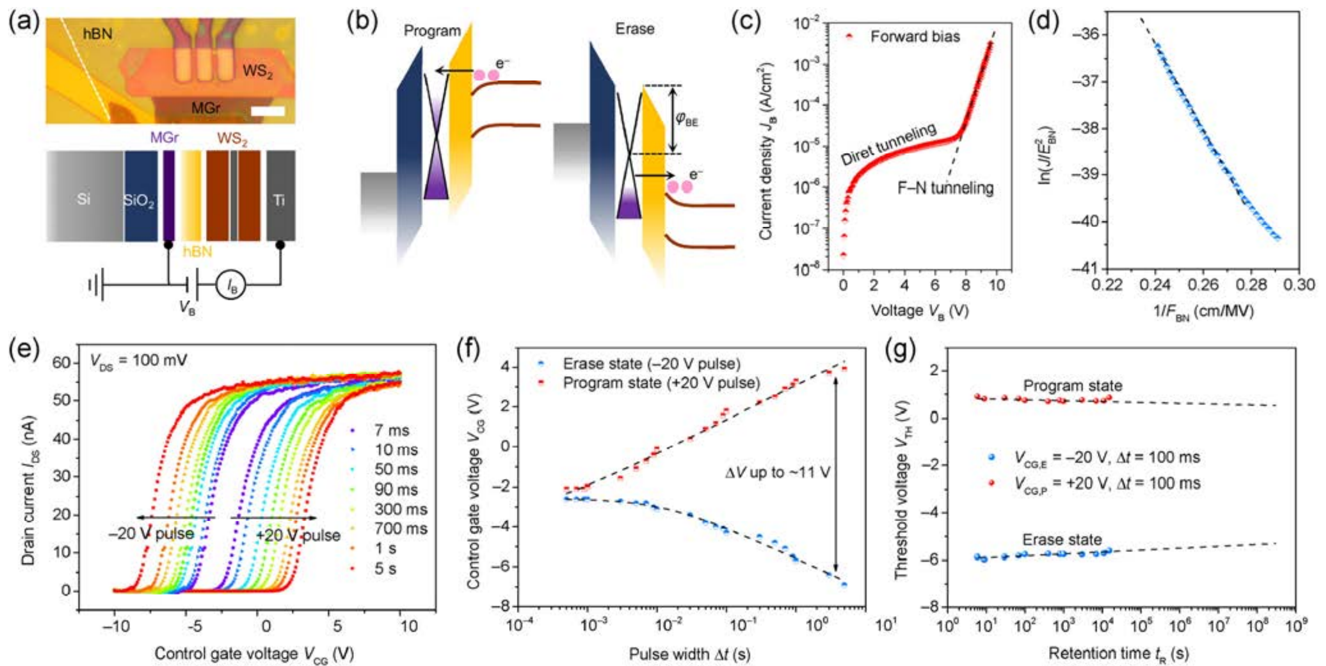

Figure 4 Tunneling current analysis, transient characteristics, and charge retention. (a) Top: Optical image of the Ti–WS_2–hBN–MGr–Ti device (the scale bar is 10 μm). The thickness of WS_2 and hBN were 9.4 and 21 nm, respectively. Bottom: schematics of the measurement setup for measuring electrical conduction in the hBN barrier. Here, $J_B = I_B/A$, with an active contact area A. (b) Energy band diagram of floating-gate memories in the program ($V_{CG} > 0$) and erase operation ($V_{CG} < 0$). Here, ϕ_{BE} represents the tunnel barrier. The flat energy band structure is illustrated in Section S9 in the ESM. (c) The measured tunneling current density J_B as a function of the applied voltage V_B for the forward direction (positive voltage on WS_2). (d) F–N plot of the measured current density. (e) Transient characteristics of the memory device when applying $V_{CG,P}$ = +20 V and $V_{CG,E}$ = −20 V pulses with various values of Δt. (f) Separation of relative control gate voltages in the programmed and erased states as a function of the pulse duration time. Data extracted from (e). (g) Charge-retention properties in each state after performing ±20 V, Δt = 100 ms pulses.

$e\phi_{BE} \approx 3.0$ eV, which is closer to the barrier height at SiO_2–Si (3.1 eV) and is also in agreement with recent theoretical calculations (namely, ~3.33 eV [42] or >4 eV [43]). This high ϕ_{BE} value significantly impacts the retention characteristics via the relationship of $t_R \propto 1/\exp(e\phi_{BE}/k_BT)$, where k_B is the Boltzmann's constant [44]. The related discussion will be presented in the last section.

2.4 Transient programming and erasing properties

Next, The transient characteristics of the floating-gate memories were evaluated. The capability of charge trapping and releasing manifested by employing V_{CG} = ±20 V with a different Δt, typically in the 10 μs–5 s range. For monitoring the associated device states, we measured the transfer characteristics with different sweeping directions, i.e., −10 to +10 V for the erased state and +10 to −10 V for the programmed state. These measurement procedures minimize the influence of V_{TH}. Figure 4(e) displays a series of I_{DS}–V_{CG} curves acquired for $V_{CG,E}$ = −20 V and $V_{CG,P}$ = +20 V. The corresponding plot of ΔV as a function of Δt is presented in Fig. 4(f). One of the characterized variables is ΔV, which exceeded 2.7 V for Δt = 5 ms and 11 V for 5 s. Moreover, the charge trapping and detrapping rates were proportional to $\Delta V/\Delta t$, implying a large electron transportation tunnel through hBN with a high traveling velocity (~10^7 cm/s) in the conduction band of the dielectric [35]. This carrier injection was governed by either direct tunneling or F–N tunneling, which is further clarified by the temperature dependent I_B–V_B measurements (Section S7 in the ESM). The electric field in the two insulators (SiO_2 and hBN) was then considered. Because of their similar dielectric constants of ~4, the electric field in each insulator was equal to the initial state of the devices (assuming that no electrons are stored on the floating-gate), i.e., $F_{BN} = F_{OX}$. Therefore, the injection field at a given value of V_{CG}

can be estimated as $F_{BN} = V_{CG}/(d_{OX} + d_{BN}) \approx 7 \times 10^5$ V/cm at V_{CG} = 20 V, where d_{OX} and d_{BN} are the thickness of SiO_2 and hBN, respectively. However, F–N tunneling occurs beyond the electric field of approximately 3 MV/cm, based on the experimental observations (Fig. 4(c)), demonstrating that our devices operated in direct-tunneling mode (Fig. 4(b)), which is consistent with that of other reports [7].

One benefit of using MGr instead of graphene is the high capacity of the charge storage, as the density of states of MGr is at least five-fold greater than that of graphene [26], which produces a large value of ΔV. The trapped charge density n in the floating-gate can be obtained using $n = \Delta V \varepsilon_{BN} \varepsilon_0 / e d_{OX}$, where ε_0 is the permittivity of the vacuum. Therefore, the charge density can be estimated as 8.48×10^{11} cm^{-2} at ΔV = 11 V.

2.5 Charge retention characteristics

The ability to retain valid data over a long period of time was examined by monitoring the shift of V_{TH} for each on and off state. As presented in Fig. 4(g), after a $V_{CG,P}$ = +20 V and Δt = 100 ms pulse was applied to the control gate, a programmed state was identified. Then, the I_{DS}–V_{CG} transfer curve was acquired from the reverse direction of the voltage sweep (+10 to −10 V) at V_{DS} = 100 mV. On the other hand, the erased state was obtained using $V_{CG,E}$ = −20 V with the same pulse duration; the variation of V_{TH} was monitored via the forward voltage sweep (−10 to +10 V). In both of the device states, the transfer characteristics were studied at different time intervals (a range from 6 s up to 15,000 s), as shown in Fig. S8 in the ESM. ΔV was reduced from 6.8 to 6.4 V over a time of 15,000 s. By linearly fitting the extracted V_{TH} values in both states, we are able to estimate the reduced ΔV as 5.9 V after 10 years. Therefore, our devices would retain ~87% of the initial charge (only 13% charge loss) on the embedded MGr after 10 years of retention. Remarkably, this dramatic enhancement of the retention was recorded as 2- to 3-fold smaller than that of reported MoS_2 memories, which commonly have 28%–40% charge loss after 10 years [9–11]. Furthermore, even over the order of centuries (10^9 s), t_R is expected to avoid significant degradation, which is comparable performance to that of silicon-based single-ploy floating-gate cells [35]. The high performance of the retention characteristics implies that only limited leakage paths contribute to charge loss.

3 Conclusions

In summary, we realized non-volatile memory devices using WS_2 as a semiconducting channel and based entirely on 2D crystals in the architecture. The memory devices encapsulate multi-layered graphene in the gate dielectric and demonstrated a high on-/off-state ratio greater than 10^3 and a large memory window of approximately 20 V. More importantly, the tunnel barrier height was greater than 3 eV at the MGr–hBN interface, leading to reliable charge retention of ~13% charge loss after 10 years. This study offers a new device architecture for achieving future nanoelectronic building blocks by utilizing atomically thin vdW stacks.

4 Experimental

The memory devices were created using scotch-tape-based cleavage of bulk graphite. A relatively thick graphene layer was initially deposited on a SiO_2 (280 nm)/Si substrate, onto which an indicator metal pad was pre-deposited. This indicator pad was typically electrically disconnected from the main body of the memory devices and served as an optical guide for mechanically-exfoliated MGr transfer. The transfer technique of the 2D crystals used a viscoelastic PDMS interlayer, similar to our previous studies [29, 45]. Other 2D crystals, such as hBN and WS_2, were also positioned on the substrate using the same method. A step-by-step fabrication procedure for the vdW heterostructure is shown in Section S1 in the ESM. A focused ion beam (FEI, Quanta 3D FEG) was used to prepare site-specific samples for cross-sectional TEM measurements after sputtering of the Pt-carbon protective layer. TEM analysis was performed using a JEOL JEM-2100F operating at 200 kV and equipped with an EDX detector. Topographic images were obtained using an AFM (Park systems, XE-100) operated in the non-contact mode with Nanosensor AR5-NCH cantilevers. Raman analyses were performed using

confocal Raman spectroscopy (WiTec, alpha 300) with laser excitation at λ = 488 nm. The electrical characterizations of the memory device were conducted with a pulse generator expander (HP, 41501A) attached to a semiconductor parameter analyzer (HP, 4156A) in a cryostat (ASK, 700K) with a base pressure of ~2 × 10^{-3} Torr at room temperature.

Acknowledgements

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Electronic Supplementary Material: Supplementary material (detailed fabrication of the devices, material characterization, hysteresis characteristics, WS_2 FET with an hBN substrate, additional data for retention performance, and temperature dependent *I–V* measurements) is available in the online version of this article at http://dx.doi.org/10.1007/s12274-016-1118-6.

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